

# TA8435H

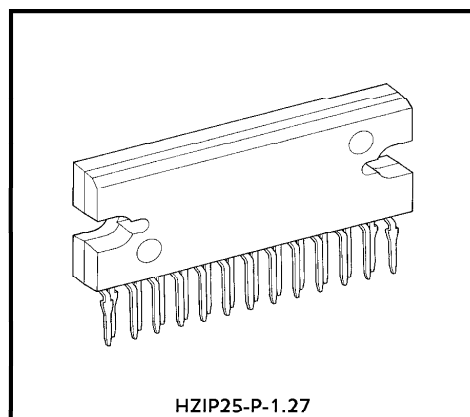
## PWM CHOPPER TYPE BIPOLAR STEPPING MOTOR DRIVER.

The TA8435H is PWM chopper type sinusoidal micro step bipolar stepping motor driver.

Sinusoidal micro step operation is accomplished only a clock signal inputting by means of built-in hard ware.

### FEATURES

- 1 chip bipolar sinusoidal micro step stepping motor driver.
- Output current up to 1.5A (AVE.) and 2.5A (PEAK).
- PWM chopper type.
- Structured by high voltage Bi-CMOS process technology.
- Forward and reverse rotation are available.
- 2, 1-2, W1-2, 2W1-2 phase 1 or 2 clock drives are selectable.
- Package : HZIP25-P
- Input Pull-up Resistor equipped with  $\overline{\text{RESET}}$  Terminal :  $R = 100k\Omega$  (Typ.)
- Output Monitor available with  $\overline{\text{MO}}$ .  $I_O(\overline{\text{MO}}) = \pm 2\text{mA}$  (MAX.)
- Reset and Enable are available with  $\overline{\text{RESET}}$  and  $\overline{\text{ENABLE}}$ .



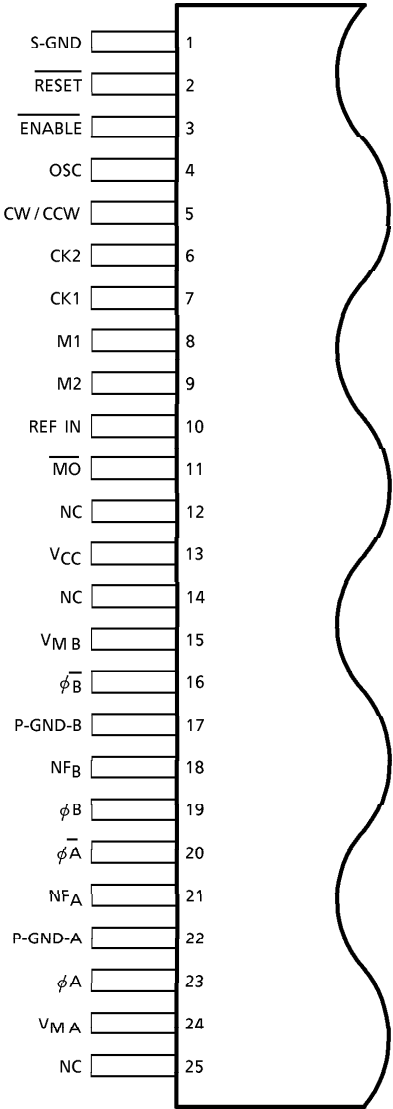
Weight : 9.86g (Typ.)

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PIN CONNECTION (Top view)

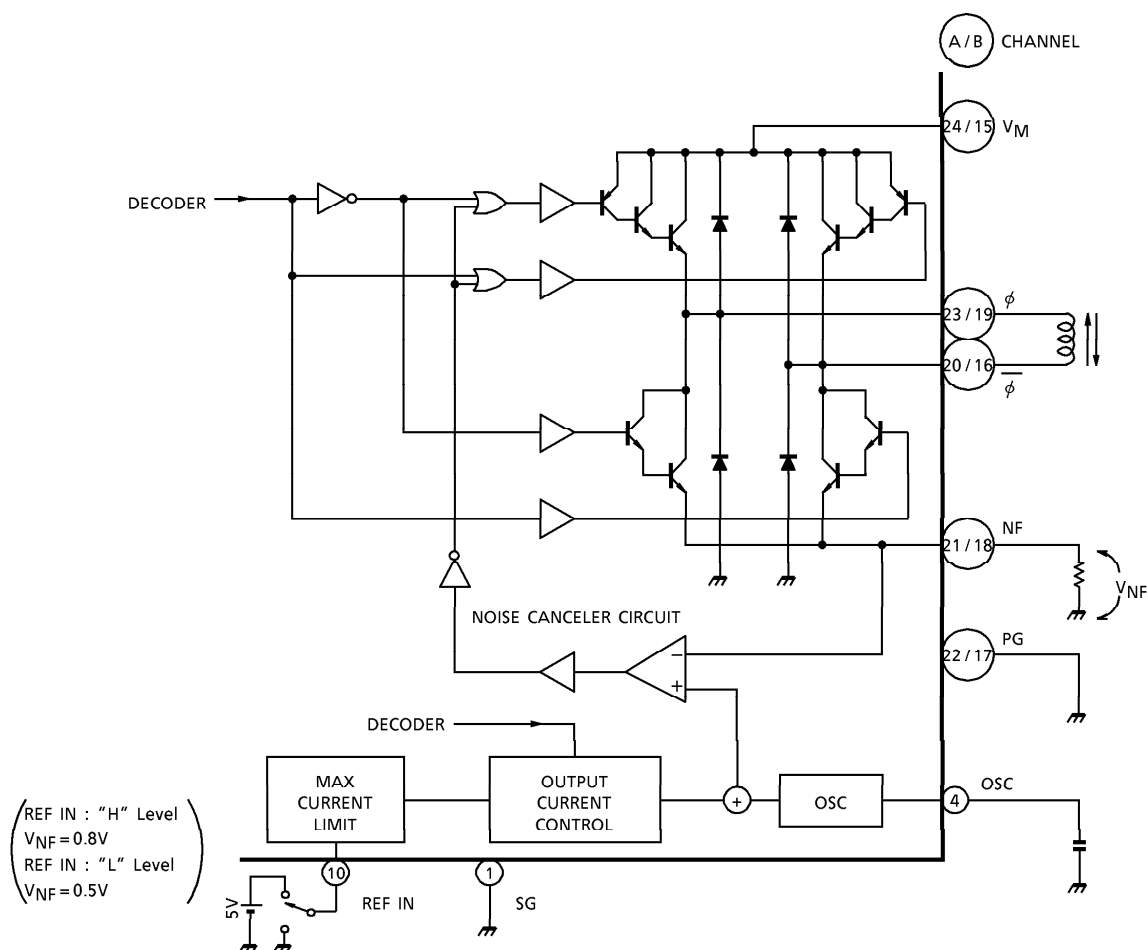


(Note) NC : No connection

## PIN FUNCTION

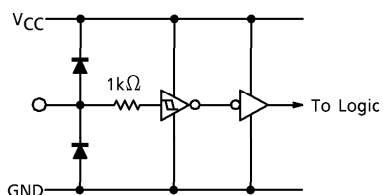
PIN No.	SYMBOL	FUNCTIONAL DESCRIPTION
1	SG	Signal GND.
2	$\overline{\text{RESET}}$	L : RESET.
3	$\overline{\text{ENABLE}}$	L : ENABLE, H : OFF.
4	OSC	Chopping oscillation is determined by the external capacitor.
5	CW / CCW	Forward / Reverse switching terminal.
6	CK2	Clock input terminal.
7	CK1	Clock input terminal.
8	M1	Excitation control input
9	M2	Excitation control input
10	REF IN	$V_{NF}$ control input
11	$\overline{\text{MO}}$	Monitor output
12	NC	No connection.
13	$V_{CC}$	Voltage supply for logic.
14	NC	No connection.
15	$V_{MB}$	Output power supply terminal.
16	$\phi\overline{B}$	Output $\phi\overline{B}$
17	PG-B	Power GND.
18	$NF_B$	B-ch output current detection terminal.
19	$\phi B$	Output $\phi B$
20	$\phi\overline{A}$	Output $\phi\overline{A}$
21	$NF_A$	A-ch output current detection terminal.
22	PG-A	Power GND
23	$\phi A$	Output $\phi A$
24	$V_{MA}$	Output power supply terminal.
25	NC	No connection.

## OUTPUT CIRCUIT

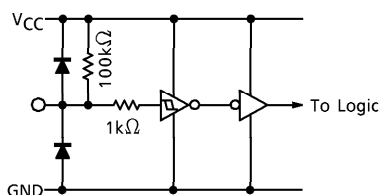


## INPUT CIRCUIT

- CK1, CK2, CW/CCW, M1, M2, REF IN : Terminals

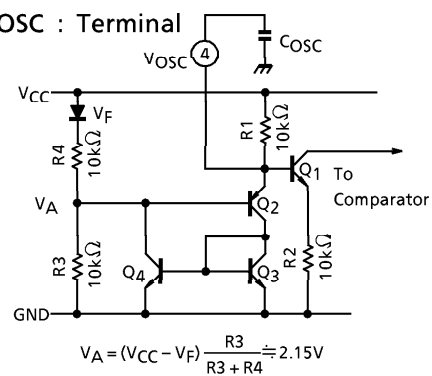


- $\overline{\text{RESET}}$ ,  $\overline{\text{ENABLE}}$  : Terminals



100kΩ of Pull-up Resistor is equipped.

- OSC : Terminal



## OSC FREQUENCY CALCULATION

Sawtooth OSC circuit consists of Q<sub>1</sub> through Q<sub>4</sub> and R1 through R4.

Q<sub>2</sub> is turned "off" when V<sub>OSC</sub> is less than the voltage of 2.5V + V<sub>BE</sub> Q<sub>2</sub> approximately equal to 2.85V.

V<sub>OSC</sub> is increased by C<sub>OSC</sub> charging through R1.

Q<sub>3</sub> and Q<sub>4</sub> are turned "on" when V<sub>OSC</sub> becomes 2.85V (Higher level.)

Lower level of V ④ pin is equal to V<sub>BE</sub> Q<sub>2</sub> + V<sub>SAT</sub> Q<sub>4</sub> approximately equal to 1.4V.

V<sub>OSC</sub> is calculated by following equation.

$$V_{OSC} = 5 \cdot \left( 1 - \exp \left( -\frac{t}{C_{OSC} \cdot R1} \right) \right) \dots\dots\dots ①$$

Assuming that V<sub>OSC</sub> = 1.4V (t = t<sub>1</sub>) and = 2.85V (t = t<sub>2</sub>)

C<sub>OSC</sub> is external capacitance connected to pin④ and R1 is on-chip 10kΩ resistor.

Therefore, OSC frequency is calculated as follows.

$$t_1 = -C_{OSC} \cdot R1 \cdot \ln \left( 1 - \frac{1.4}{5} \right) \dots\dots\dots ②$$

$$t_2 = -C_{OSC} \cdot R1 \cdot \ln \left( 1 - \frac{2.85}{5} \right) \dots\dots\dots ③$$

$$f_{OSC} = \frac{1}{t_2 - t_1} = \frac{1}{C_{OSC} \left( R1 \cdot \ln \left( 1 - \frac{1.4}{5} \right) - R1 \cdot \ln \left( 1 - \frac{2.85}{5} \right) \right)}$$

$$= \frac{1}{5.15 \cdot C_{OSC}} \text{ (kHz) } (C_{OSC} : \mu\text{F})$$

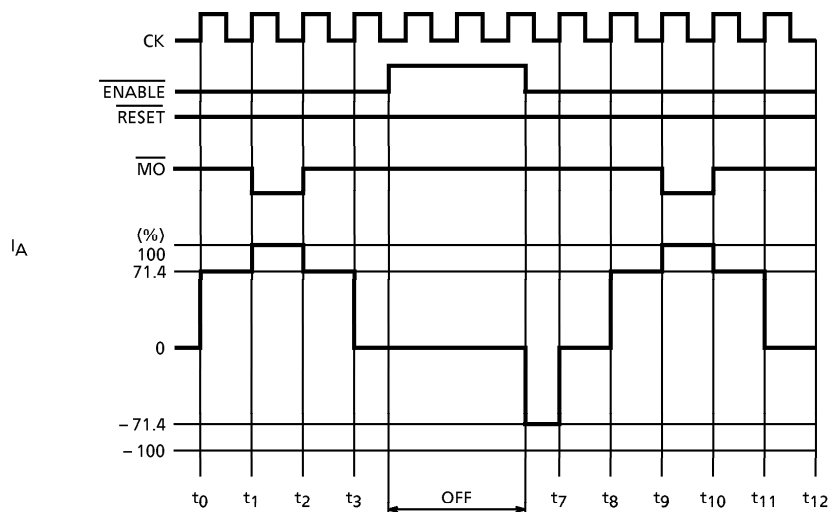
**ENABLE AND RESET FUNCTION AND  $\overline{MO}$  SIGNAL**

Fig.1 1-2 Phase drive mode (M1 : H, M2 : L)

$\overline{ENABLE}$  Signal disables only Output Signal.

Internal logic functions are proceeded by CK signal without regard to  $\overline{ENABLE}$  signal.

Therefore, Output Current is initiated from the proceeded timing point of internal logic circuit after release of disable mode.

Fig.1 shows the  $\overline{ENABLE}$  functions, when the system is selected in 1-2 Phase drive mode.

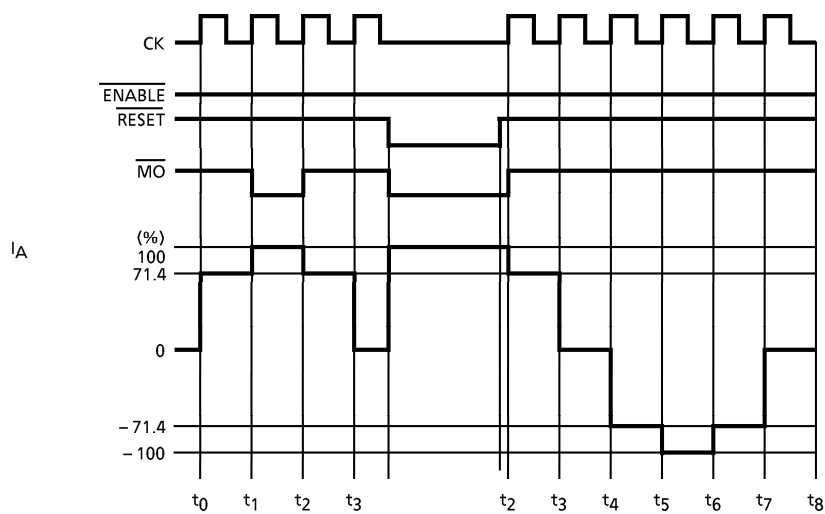


Fig.2 1-2 Phase drive mode (M1 : H, M2 : L)

Low level active of  $\overline{RESET}$  Signal offs not only the Outputs but also stops internal CK functions and  $\overline{MO}$  to low.

Outputs are initiated from the initial point after release of  $\overline{RESET}$  (High) as shown in Fig.2.

$\overline{MO}$  (Monitor Output) Signals can be used as rotation and initial signal for stable rotation checking.

FUNCTION

INPUT					MODE
CK1	CK2	CW / CCW	RESET	ENABLE	
	H	L	H	L	CW
	L	L	H	L	INHIBIT (Note)
H		L	H	L	CCW
L		L	H	L	INHIBIT (Note)
	H	H	H	L	CCW
	L	H	H	L	INHIBIT (Note)
H		H	H	L	CW
L		H	H	L	INHIBIT (Note)
X	X	X	L	L	RESET
X	X	X	X	H	Z

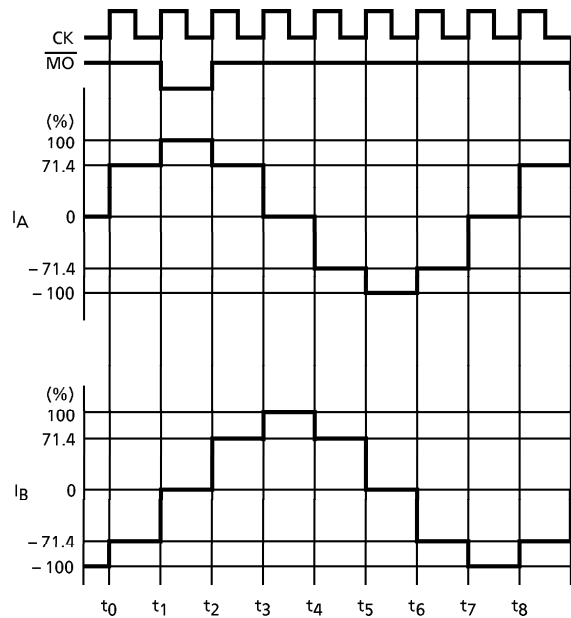
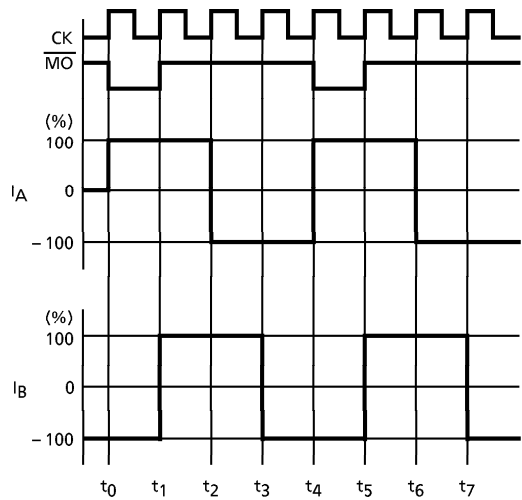
INITIAL MODE

EXCITATION MODE	A PHASE CURRENT	B PHASE CURRENT
2 Phase	100%	– 100%
1-2 Phase	100%	0%
W1-2 Phase	100%	0%
2W1-2 Phase	100%	0%

Z : High impedance  
X : Don't Care

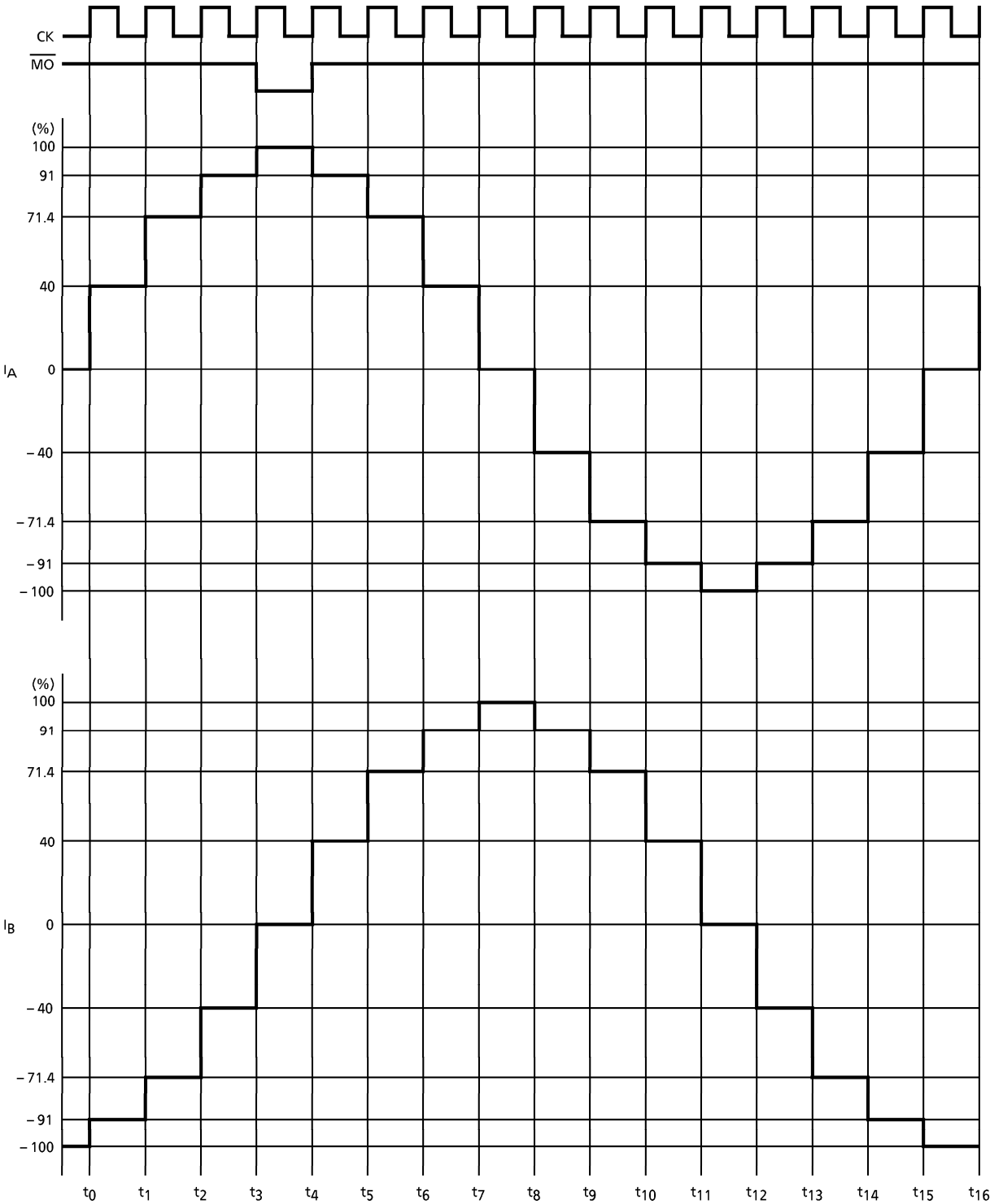
INPUT		MODE (EXCITATION)
M1	M2	
L	L	2 Phase
H	L	1-2 Phase
L	H	W1-2 Phase
H	H	2W1-2 Phase

2 PHASE EXCITATION (M1 : L, M2 : L, CW MODE) 1-2 PHASE EXCITATION (M1 : H, M2 : L, CW MODE)

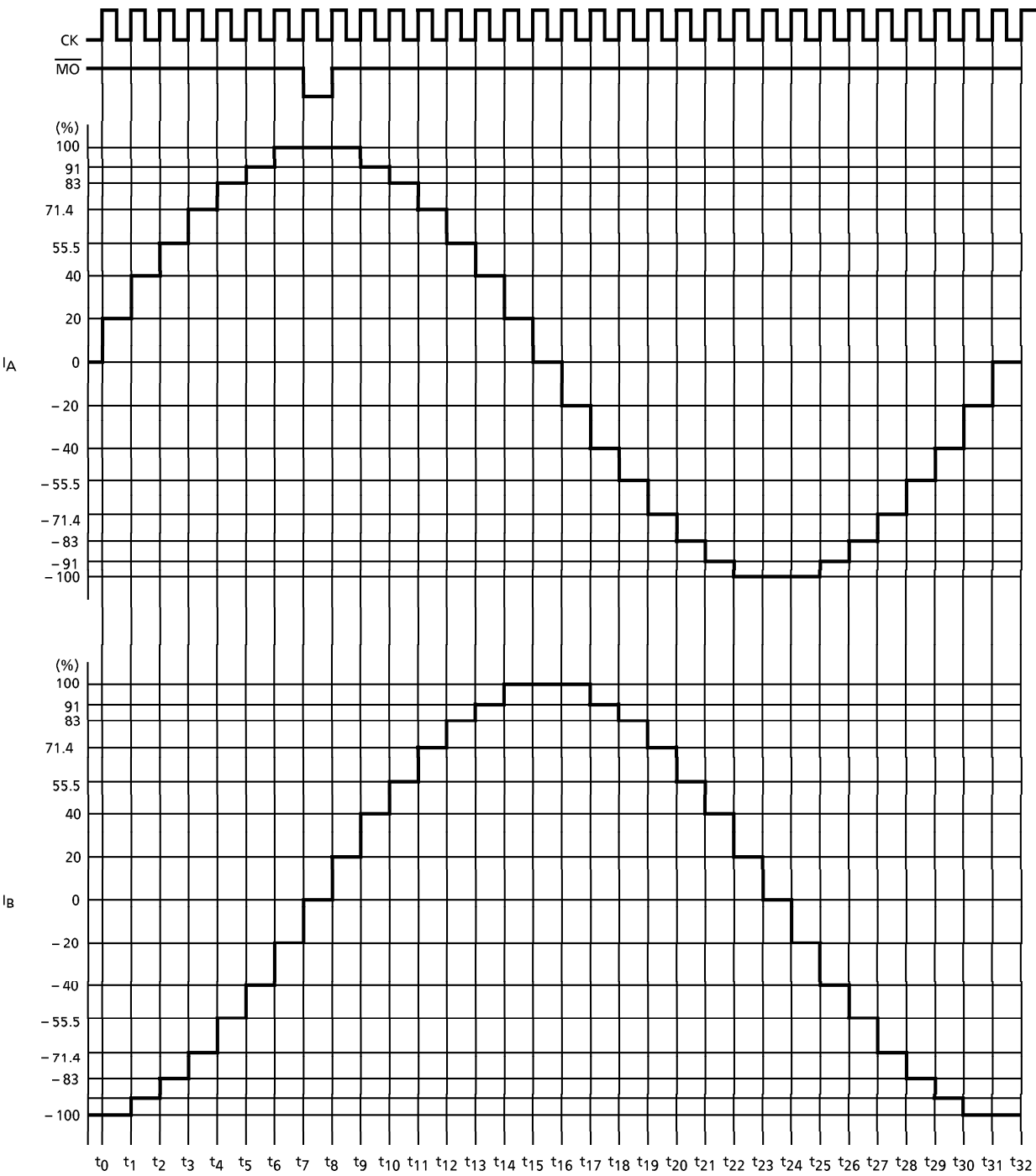




W1-2 PHASE EXCITATION (M1 : L, M2 : H, CW MODE)



2W1-2 PHASE EXCITATION (M1 : H, M2 : H, CW MODE)



**MAXIMUM RATINGS** (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V <sub>CC</sub>	5.5	V
Output Voltage		V <sub>M</sub>	40	V
Output Current	PEAK	I <sub>O</sub> (PEAK)	2.5	A
	AVE.	I <sub>O</sub> (AVE.)	1.5	
$\overline{M}\overline{O}$ Output Current		I <sub>O</sub> ( $\overline{M}\overline{O}$ )	± 2	mA
Input Voltage		V <sub>IN</sub>	~V <sub>CC</sub>	V
Power Dissipation		P <sub>D</sub>	5 (Note 1)	W
			43 (Note 2)	
Operating Temperature		T <sub>opr</sub>	– 40~85	°C
Storage Temperature		T <sub>stg</sub>	– 55~150	°C
Feed Back Voltage		V <sub>NF</sub>	1.0	V

(Note 1) No heat sink

(Note 2) T<sub>c</sub> = 85°C**RECOMMENDED OPERATING CONDITIONS** (Ta = – 20~75°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V <sub>CC</sub>	—	4.5	5.0	5.5	V
Output Voltage	V <sub>M</sub>	—	21.6	24	26.4	V
Output Current	I <sub>OUT</sub>	—	—	—	1.5	A
Input Voltage	V <sub>IN</sub>	—	—	—	V <sub>CC</sub>	V
Clock Frequency	f <sub>CK</sub>	—	—	—	5	kHz
OSC Frequency	f <sub>OSC</sub>	—	15	—	80	kHz

ELECTRICAL CHARACTERISTICS (Ta = 25°C, V<sub>CC</sub> = 5V, V<sub>M</sub> = 24V)

CHARACTERISTIC		SYMBOL	TEST CIRCUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Input Voltage	High	V <sub>IN</sub> (H)	1	M1, M2, CW / CCW, REF IN ENABLE, CK1, CK2 RESET		3.5	—	V <sub>CC</sub> + 0.4	V
	Low	V <sub>IN</sub> (L)				GND – 0.4	—	1.5	
Input Hysteresis Voltage		V <sub>H</sub>							—
Input Current		I <sub>IN</sub> -1 (H)	1	M1, M2, REF IN, V <sub>IN</sub> = 5.0V		—	—	100	nA
		I <sub>IN</sub> -1 (L)		RESET, ENABLE, V <sub>IN</sub> = 0V, INTERNAL PULL-UP RESISTOR		10	50	100	μA
		I <sub>IN</sub> -2 (L)		SOURCE TYPE, V <sub>IN</sub> = 0V		—	—	100	nA
Quiescent Current V <sub>CC</sub> Terminal		I <sub>CC</sub> 1	1	Output Open, RESET : H, ENABLE : L (2, 1-2 Phase excitation)		—	10	18	mA
		I <sub>CC</sub> 2		Output Open, RESET : H, ENABLE : L (W1-2, 2W1-2 Phase excitation)		—	10	18	
		I <sub>CC</sub> 3		RESET : L, ENABLE : H		—	5	—	
		I <sub>CC</sub> 4		RESET : H, ENABLE : H		—	5	—	
Comparator Reference Voltage	High	V <sub>NF</sub> (H)	3	REF IN H Output Open	(Note)	0.72	0.8	0.88	V
	Low	V <sub>NF</sub> (L)		REF IN L Output Open		0.45	0.5	0.55	
Output Differential		ΔV <sub>O</sub>	—	B / A, C <sub>OSC</sub> = 0.0033 μF, R <sub>NF</sub> = 0.8Ω		– 10	—	10	%
V <sub>NF</sub> (H) – V <sub>NF</sub> (L)		ΔV <sub>NF</sub>	—	V <sub>NF</sub> (L) / V <sub>NF</sub> (H) C <sub>OSC</sub> = 0.0033 μF, R <sub>NF</sub> = 0.8Ω		56	63	70	%
NF Terminal Current		I <sub>NF</sub>	—	SOURCE TYPE		—	170	—	μA
Maximum OSC Frequency		f <sub>OSC</sub> (MAX.)	—	—		100	—	—	kHz
Minimum OSC Frequency		f <sub>OSC</sub> (MIN.)	—	—		—	—	10	kHz
OSC Frequency		f <sub>OSC</sub>	—	C <sub>OSC</sub> = 0.0033 μF		25	44	62	kHz
Minimum Clock Pulse Width		t <sub>W</sub> (CK)	—	—		—	1.0	—	μs
Output Voltage		V <sub>OH</sub> (MO)	—	I <sub>OH</sub> = – 40 μA		4.5	4.9	V <sub>CC</sub>	V
		V <sub>OL</sub> (MO)		I <sub>OL</sub> = 40 μA		GND	0.1	0.5	

(Note) 2 Phase excitation, R<sub>NF</sub> = 0.7 Ω, C<sub>OSC</sub> = 0.0033 μF

## OUTPUT BLOCK

CHARACTERISTIC				SYMBOL	TEST CIR- CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Output Saturation Voltage	Upper Side			V <sub>SAT</sub> U1	4	I <sub>OUT</sub> = 1.5A	—	2.1	2.8	V	
	Lower Side			V <sub>SAT</sub> L1			—	1.3	2.0		
	Upper Side			V <sub>SAT</sub> U2		I <sub>OUT</sub> = 0.8A	—	1.8	2.2		
	Lower Side			V <sub>SAT</sub> L2			—	1.1	1.5		
	Upper Side			V <sub>SAT</sub> U3		I <sub>OUT</sub> = 2.5A Pulse width 30ms	—	2.5	3.0		
	Lower Side			V <sub>SAT</sub> L3			—	1.8	2.2		
Diode Forward Voltage	Upper Side			V <sub>F</sub> U1	5	I <sub>OUT</sub> = 1.5A	—	2.0	3.0	V	
	Lower Side			V <sub>F</sub> L1			—	1.5	2.1		
	Upper Side			V <sub>F</sub> U2		I <sub>OUT</sub> = 2.5A Pulse width 30ms	—	2.5	3.3		
	Lower Side			V <sub>F</sub> L2			—	1.8	2.5		
Output Dark Current (A + B Channels)				I <sub>M1</sub>	2	ENABLE : "H" Level, Output Open RESET : "L" Level	—	—	50	μA	
				I <sub>M2</sub>		ENABLE : "L" Level Output Open RESET : "H" Level	—	8	15	mA	
A-B Chopping Current (Note)	2W1-2ϕ	W1-2ϕ	1-2ϕ	VECTOR	—	θ = 0	REF IN : H R <sub>NF</sub> = 0.8Ω C <sub>OSC</sub> = 0.0033μF	—	100	—	%
	2W1-2ϕ	—	—			θ = 1 / 8		—	100	—	
	2W1-2ϕ	W1-2ϕ	—			θ = 2 / 8		86	91	96	
	2W1-2ϕ	—	—			θ = 3 / 8		78	83	88	
	2W1-2ϕ	W1-2ϕ	1-2ϕ			θ = 4 / 8		66.4	71.4	76.4	
	2W1-2ϕ	—	—			θ = 5 / 8		50.5	55.5	60.5	
	2W1-2ϕ	W1-2ϕ	—			θ = 6 / 8		35	40	45	
	2W1-2ϕ	—	—			θ = 7 / 8		15	20	25	
	2 Phase Excitation Mode VECTOR					—		—	100	—	

(Note) Maximum current ( $\theta = 0$ ) : 100%2W1-2 $\phi$  : 2W1, 2 phase excitation modeW1-2 $\phi$  : W1, 2 phase excitation mode1-2 $\phi$  : 1, 2 phase excitation mode

CHARACTERISTIC				SYMBOL	TEST CIR- CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
A-B Chopping Current (Note)	2W1-2 $\phi$	W1-2 $\phi$	1-2 $\phi$	VECTOR	—	$\theta = 0$	REF IN : L $R_{NF} = 0.8\Omega$ $C_{OSC} = 0.0033\mu F$	—	100	—	%
	2W1-2 $\phi$	—	—			$\theta = 1/8$		—	100	—	
	2W1-2 $\phi$	W1-2 $\phi$	—			$\theta = 2/8$		86	91	96	
	2W1-2 $\phi$	—	—			$\theta = 3/8$		78	83	88	
	2W1-2 $\phi$	W1-2 $\phi$	1-2 $\phi$			$\theta = 4/8$		66.4	71.4	76.4	
	2W1-2 $\phi$	—	—			$\theta = 5/8$		50.5	55.5	60.5	
	2W1-2 $\phi$	W1-2 $\phi$	—			$\theta = 6/8$		35	40	45	
	2W1-2 $\phi$	—	—			$\theta = 7/8$		15	20	25	
	2 Phase Excitation Mode VECTOR					—		—	100	—	
Feed Back Voltage Step				$\Delta V_{NF}$	—	$\Delta\theta = 0/8 - 1/8$	REF IN : H $R_{NF} = 0.8\Omega$ $C_{OSC} = 0.0033\mu F$	—	0	—	mV
						$\Delta\theta = 1/8 - 2/8$		32	72	112	
						$\Delta\theta = 2/8 - 3/8$		24	64	104	
						$\Delta\theta = 3/8 - 4/8$		53	93	133	
						$\Delta\theta = 4/8 - 5/8$		87	127	167	
						$\Delta\theta = 5/8 - 6/8$		84	124	164	
						$\Delta\theta = 6/8 - 7/8$		120	160	200	
Output $T_r$ Switching Characteristics				$t_r$	7	$R_L = 2\Omega$ , $V_{NF} = 0V$ , $C_L = 15pF$		—	0.3	—	$\mu s$
				$t_f$				—	2.2	—	
				$t_{pLH}$		CK~Output		—	1.5	—	
				$t_{pHL}$				—	2.7	—	
				$t_{pLH}$		OSC~Output		—	5.4	—	
				$t_{pHL}$				—	6.3	—	
				$t_{pLH}$		RESET~Output		—	2.0	—	
				$t_{pHL}$				—	2.5	—	
				$t_{pLH}$		ENABLE~Output		—	5.0	—	
				$t_{pHL}$				—	6.0	—	
Output Leakage Current		Upper Side	$I_{OH}$	6	$V_M = 30V$		—	—	50	$\mu A$	
		Lower Side	$I_{OL}$				—	—	50		

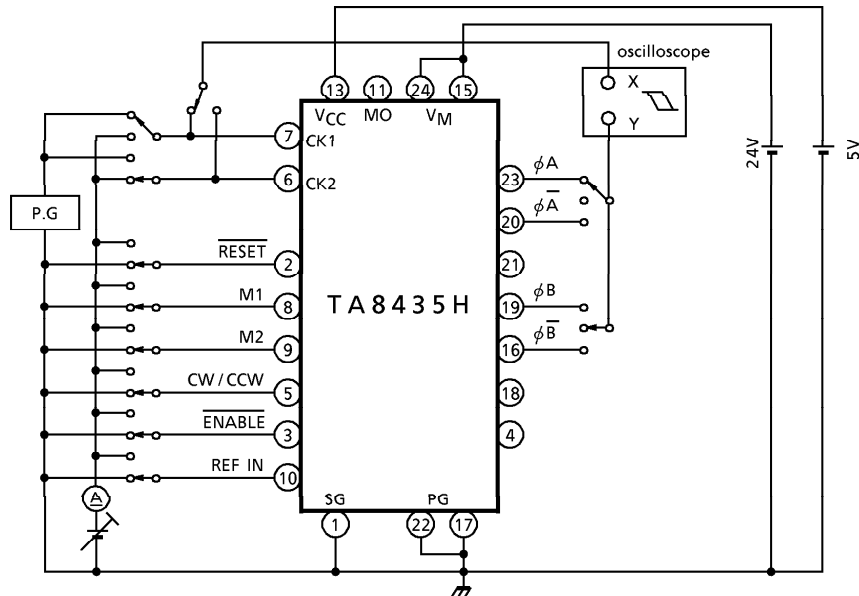
(Note) Maximum current ( $\theta = 0$ ) : 100%

2W1-2 $\phi$  : 2W1, 2 phase excitation mode

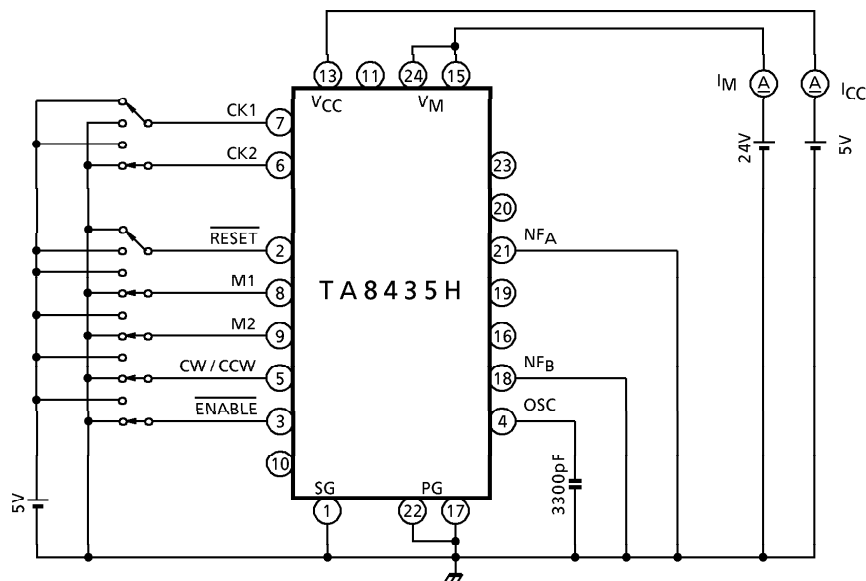
W1-2 $\phi$  : W1, 2 phase excitation mode

1-2 $\phi$  : 1, 2 phase excitation mode

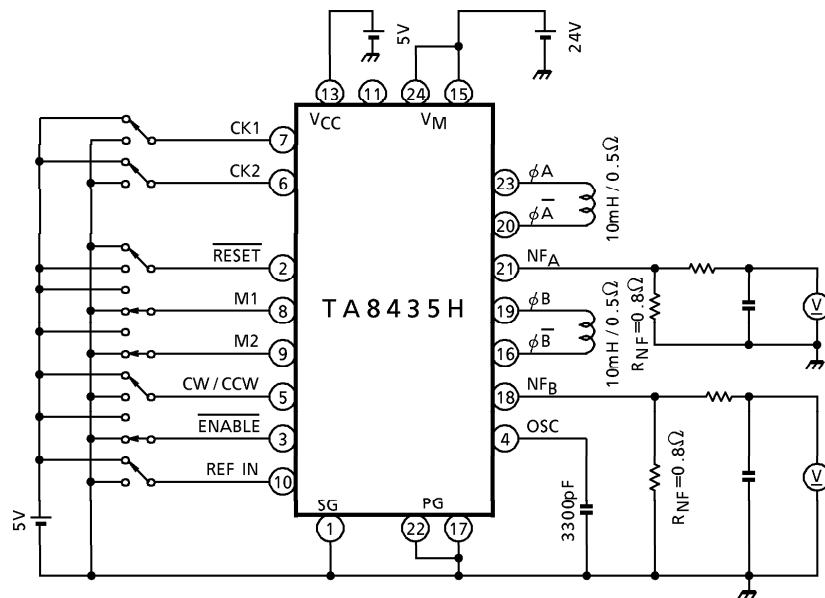
## TEST CIRCUIT 1

 $V_{IN}(H), (L), I_{IN}(H), (L)$ 

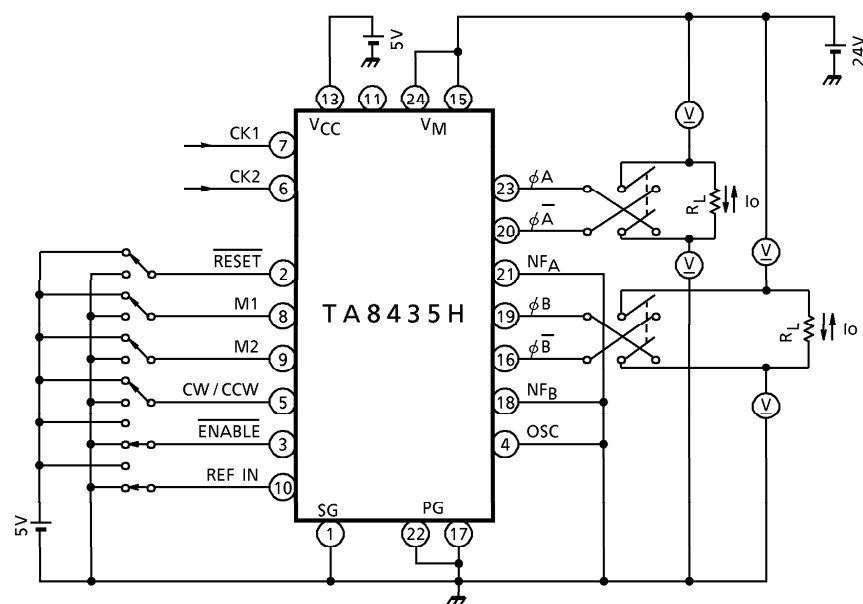
## TEST CIRCUIT 2

 $I_{CC}, I_M$ 

## TEST CIRCUIT 3

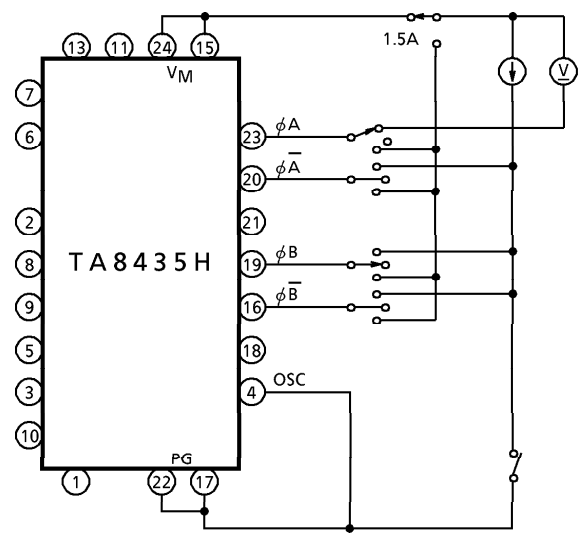
 $V_{NF(H)}, (L)$ 

## TEST CIRCUIT 4

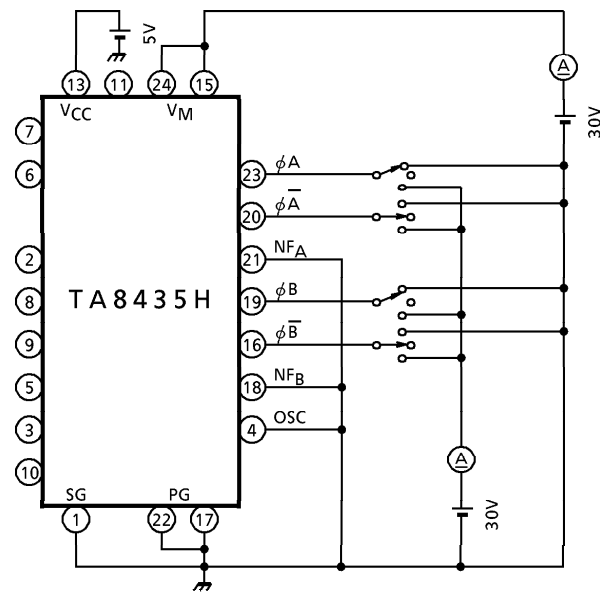
 $V_{CE(SAT)}$  UPPER SIDE, LOWER SIDE(Note) Calibrate  $I_o$  to 1.5A/0.8A by  $R_L$



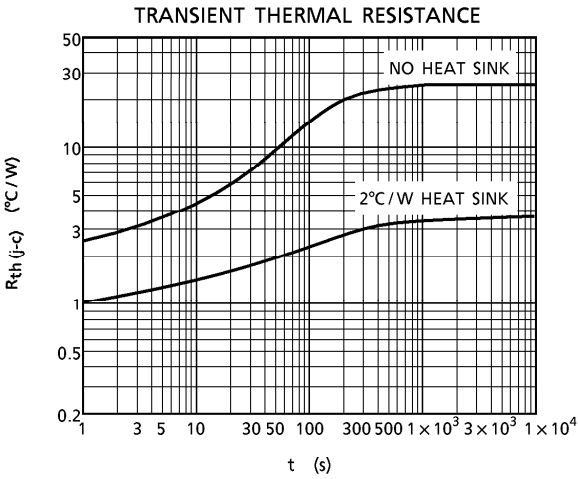
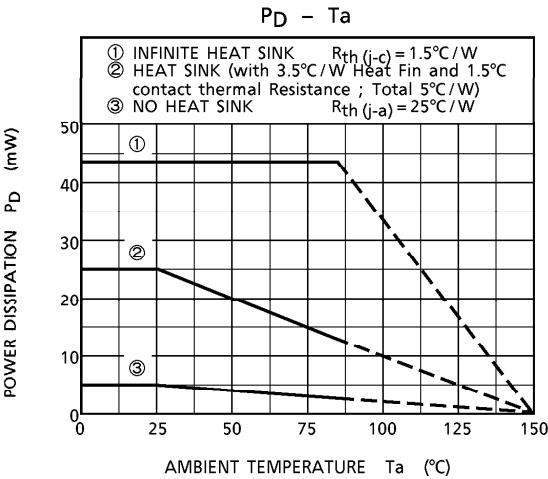
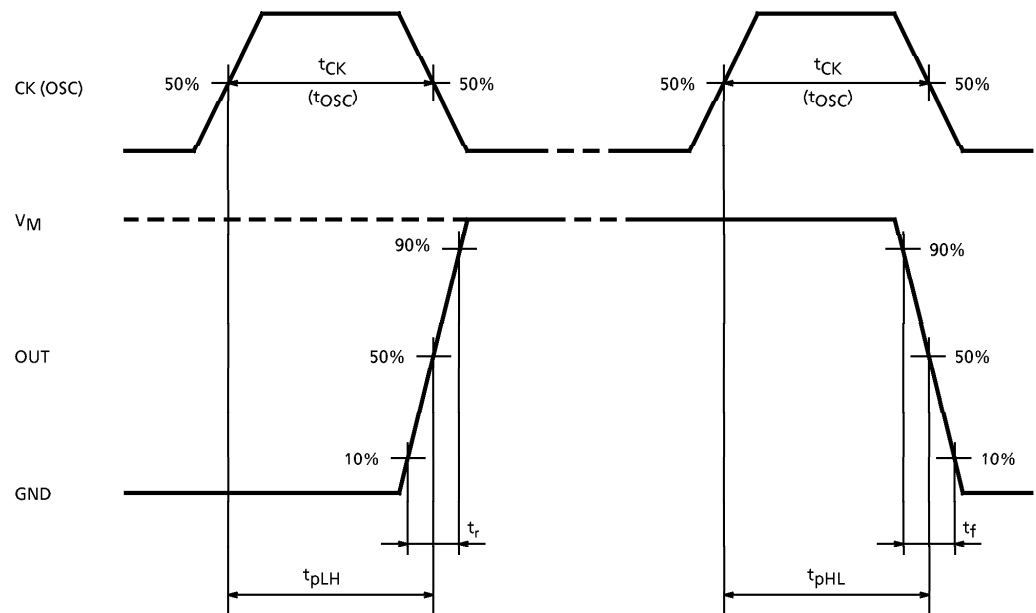
TEST CIRCUIT 5  
 $V_{FU}$ ,  $V_{FL}$



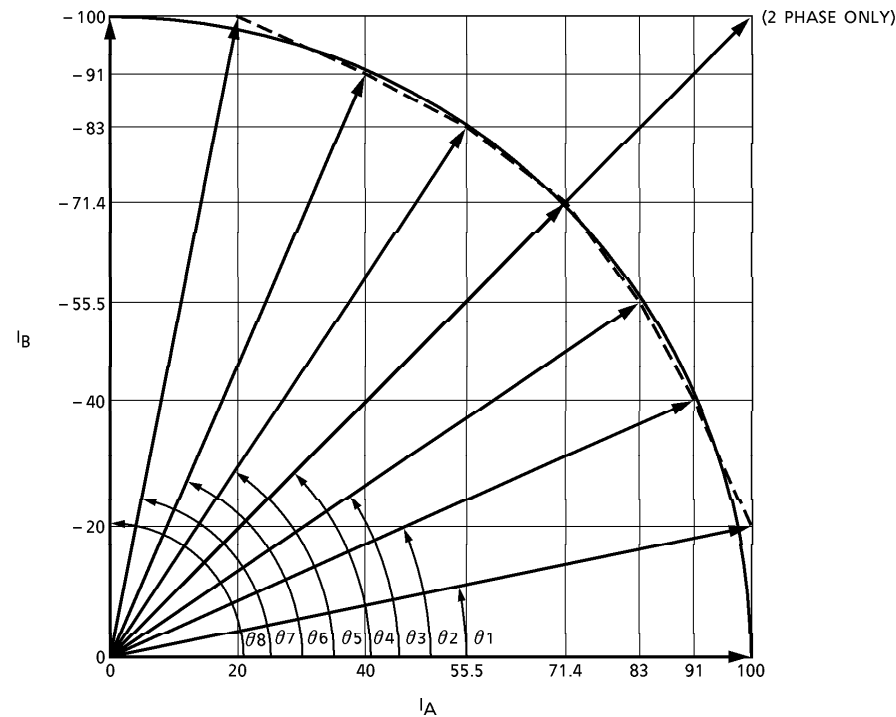
TEST CIRCUIT 6  
 $I_{OH}$ ,  $I_{OL}$



AC ELECTRICAL CHARACTERISTICS, MEASUREMENT WAVE  
CK (OSC)-OUT

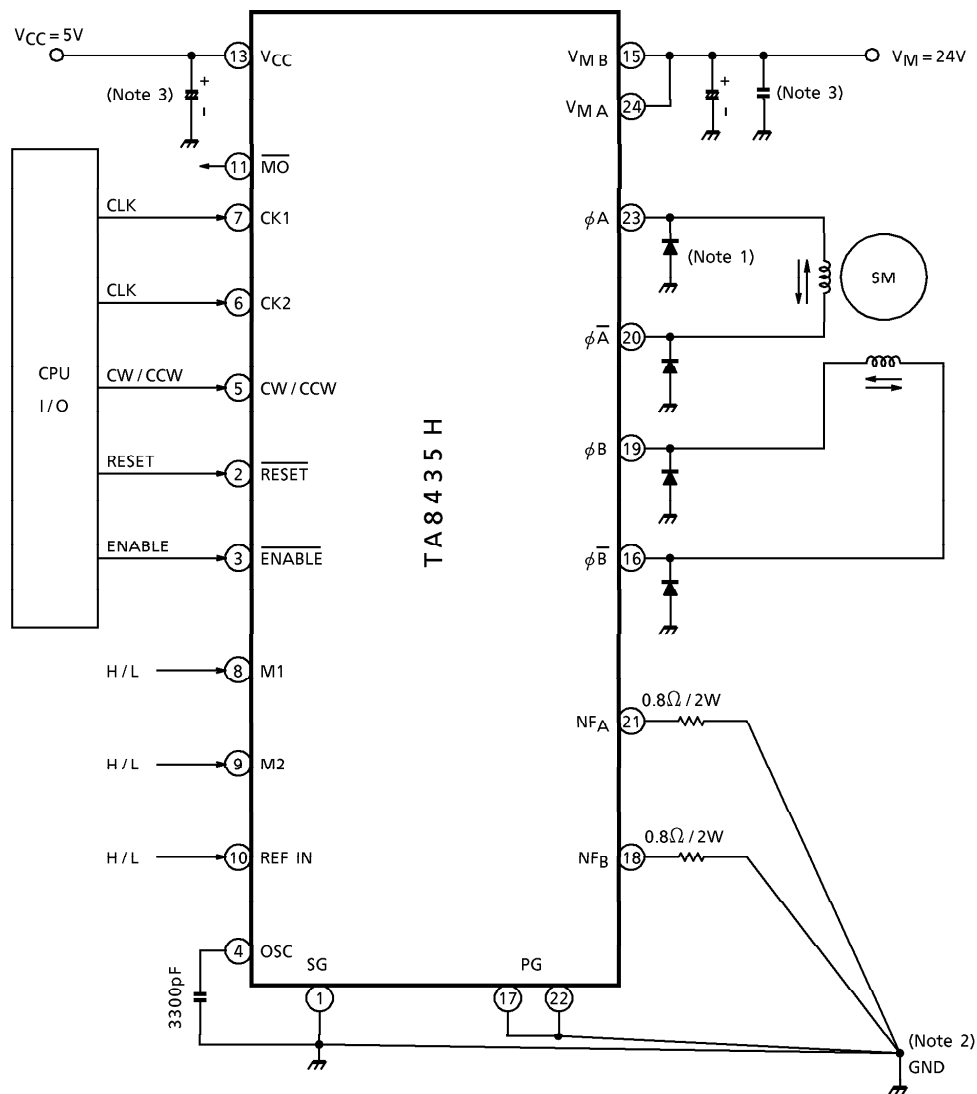


OUTPUT CURRENT VECTOR ORBIT (Normalize to 90° for each one step)



$\theta$	ROTATION ANGLE		VECTOR LENGTH		
	IDEAL	TA8435H	IDEAL	TA8435H	
$\theta_0$	0°	0°	100	100.00	—
$\theta_1$	11.25°	11.31°	100	101.98	—
$\theta_2$	22.5°	23.73°	100	99.40	—
$\theta_3$	33.75°	33.77°	100	99.85	—
$\theta_4$	45°	45°	100	100.97	141.42
$\theta_5$	56.25°	56.23°	100	99.85	—
$\theta_6$	67.5°	66.27°	100	99.40	—
$\theta_7$	78.75°	78.69°	100	101.98	—
$\theta_8$	90°	90°	100	100.00	—
			1-2 / W1-2 / 2W1-2 Phase		2 Phase

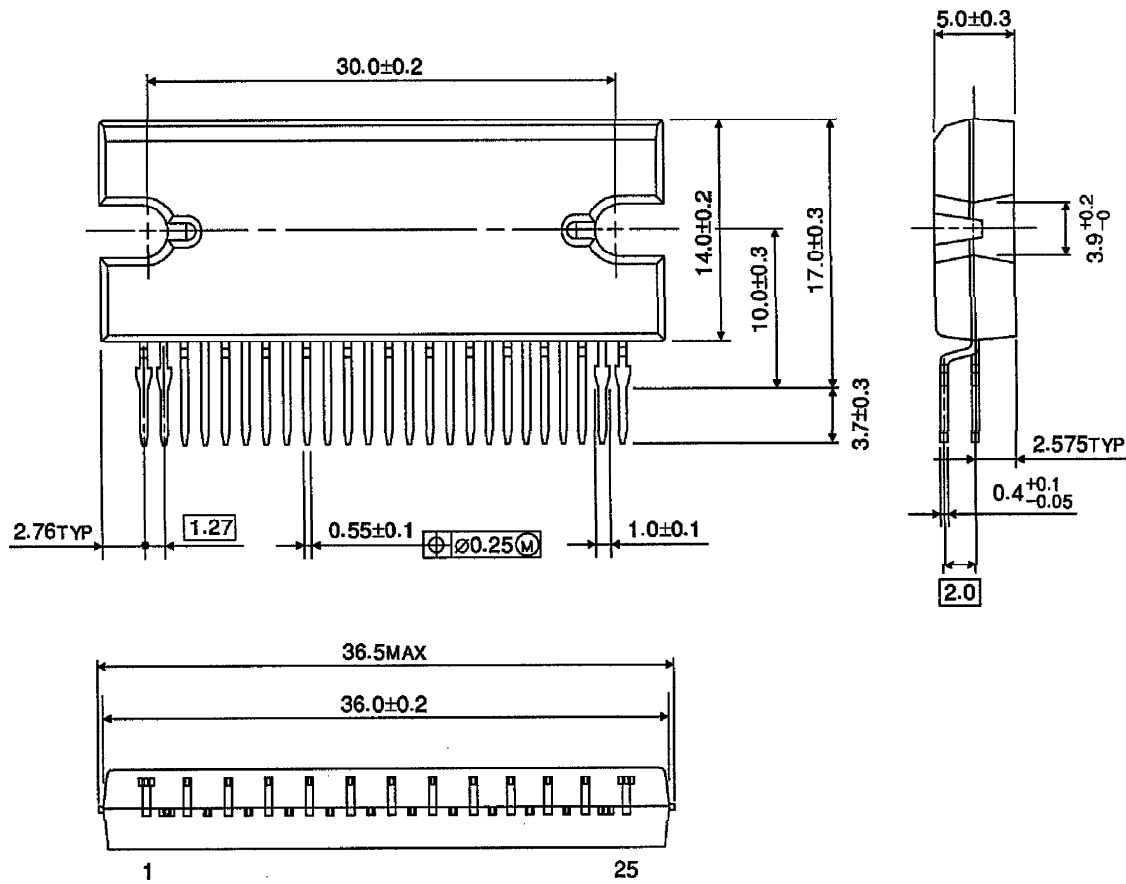
## APPLICATION CIRCUIT



- (Note 1) Schottky diode (3GWJ42) to be connected additionally between each output (pin 16/19/20/23) and GND for preventing Punch-Through Current
- (Note 2) GND pattern to be laid out at one point in order to prevent common impedance.
- (Note 3) Capacitor for noise suppression to be connected between the Power Supply ( $V_{CC}$ ,  $V_M$ ) and GND to stabilize the operation.
- (Note 4) Utmost care is necessary in the design of the output line,  $V_M$  and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

OUTLINE DRAWING  
HZIP25-P-1.27

Unit : mm



Weight : 9.86g (Typ.)